COMPILER DESIGN

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INTENDED AUDIENCE : Undergraduate students of CSE, IT, B.Sc (Computer Science), MCA, MS (Computer Science)

INDUSTRIES APPLICABLE TO : All software industries

COURSE OUTLINE :

Compilers have become part and parcel of today's computer systems. They are responsible for making the user's computing requirements, specified as a piece of program, understandable to the underlying machine. There tools work as interface between the entities of two different domains – the human being and the machine. The actual process involved in this transformation is quite complex. Automata Theory provides the base of the course on which several automated tools can be designed to be used at various phases of a compiler. Advances in computer architecture, memory management and operating systems provide the compiler designer large number of options to try out for efficient code generation. This course on compiler design is to address all these issues, starting from the theoretical foundations to the architectural issues to automated tools. Being primarily targeted to a one-semester course for the undergraduate students, the course will follow the current GATE syllabus, enabling the students to prepare well for the same. It can also help all other participants looking for an introduction to the domain of compiler designs and code translators.

ABOUT INSTRUCTOR :

Prof. Santanu Chattopadhyay received his BE degree in Computer Science and Technology from Calcutta University (B.E. College) in 1990. He received M.Tech in Computer and Information Technology and PhD in Computer Science and Engineering from Indian Institute of Technology Kharagpur in 1992 and 1996, respectively. He is currently a Professor in the Department of Electronics and Electrical Communication Engineering, IIT Kharagpur. Prior to this, he had been a faculty member in the IIEST Sibpur and IIT Guwahati in the departments of Computer Science and Engineering. In both these places he has taught the subject of Compiler Design several times. His research interests include Digital Design, Embedded Systems, System-on-Chip (SoC) and Network-on-Chip (NoC) Design and Test, Power- and Thermal-aware Testing of VLSI Circuits and Systems. He has published more than 150 papers in reputed international journals and conferences. He has published several text and reference books on Compiler Design, Embedded Systems and other related areas. He is a senior member of the IEEE and an Associate Editor of IET Circuits Devices and Systems journal.

COURSE PLAN :

Week 1**:** Introduction

Week 2**:** Lexical Analysis

Week 3**:** Parsing – Part I

Week 4**:** Parsing – Part II

Week 5**:** Parsing – Part III

Week 6**:** Syntax Directed Translation

Week 7**:** Type Checking and Symbol Tables

Week 8**:** Runtime Environment Management – Part I

Week 9**:** Runtime Environment Management – Part II

Week 10**:** Intermediate Code Generation – Part I

Week 11**:** Intermediate Code Generation – Part II

Week 12**:** Intermediate Code Generation – Part III